**DMA Controller Register Specification (For 3-Channel AHB-Lite Based Burst-Mode DMA)**

**Overview**

This document specifies the **register set** required for a 3-channel DMA Controller interfaced with an AHB-Lite master. All registers are memory-mapped and accessible by the CPU.

**Register Summary**

| **Register Name** | **Address** | **Offset** | **Width** | **Use / Description** |
| --- | --- | --- | --- | --- |
| CH0\_SRC\_ADDR | 0x40000000 | 0x00 | 32 | Channel 0 Source Address |
| CH0\_DST\_ADDR | 0x40000004 | 0x04 | 32 | Channel 0 Destination Address |
| CH0\_TRANS\_SIZE | 0x40000008 | 0x08 | 32 | Channel 0 Word Count/Transfer Size |
| CH0\_CTRL | 0x4000000C | 0x0C | 8 | Channel 0 Control bits |
| CH0\_STATUS | 0x40000010 | 0x10 | 8 | Channel 0 Status |
| CH0\_INT | 0x40000014 | 0x14 | 3 | Channel 0 Interrupt Control/Status |
| CH1\_SRC\_ADDR | 0x40000018 | 0x18 | 32 | Channel 1 Source Address |
| CH1\_DST\_ADDR | 0x4000001C | 0x1C | 32 | Channel 1 Destination Address |
| CH1\_TRANS\_SIZE | 0x40000020 | 0x20 | 32 | Channel 1 Word Count/Transfer Size |
| CH1\_CTRL | 0x40000024 | 0x24 | 8 | Channel 1 Control bits |
| CH1\_STATUS | 0x40000028 | 0x28 | 8 | Channel 1 Status |
| CH1\_INT | 0x4000002C | 0x2C | 3 | Channel 1 Interrupt Control/Status |
| CH2\_SRC\_ADDR | 0x40000030 | 0x30 | 32 | Channel 2 Source Address |
| CH2\_DST\_ADDR | 0x40000034 | 0x34 | 32 | Channel 2 Destination Address |
| CH2\_TRANS\_SIZE | 0x40000038 | 0x38 | 32 | Channel 2 Word Count/Transfer Size |
| CH2\_CTRL | 0x4000003C | 0x3C | 8 | Channel 2 Control bits |
| CH2\_STATUS | 0x40000040 | 0x40 | 8 | Channel 2 Status |
| CH2\_INT | 0x40000044 | 0x44 | 3 | Channel 2 Interrupt Control/Status |
| DMAC\_MASK | 0x40000048 | 0x48 | 3 | Mask Register (interrupt/request mask for channels) |
| DMAC\_REQ | 0x4000004C | 0x4C | 3 | Software Transfer Request Register |
| DMAC\_CMD | 0x40000050 | 0x50 | 8 | Global DMA Commands Register |
| DMAC\_CTRL | 0x40000054 | 0x54 | 8 | Global DMA Control Register |

**1. What is "Address Offset" in the Document?**

The **address offset** for each register is the **memory-mapped location** within the DMA controller’s address space where that register resides.

This offset is used by the **AHB-Lite master or CPU** to read/write specific registers through memory-mapped I/O.

For example:

* 0x00 → **Control Register (DMA Global Control)**
* 0x10 → **Channel 0 Base Address**
* 0x14 → **Channel 0 Word Count**
* 0x18 → **Channel 0 Control**
* 0x20 → **Channel 1 Base Address**, etc.

You can think of it like this:

| **Register** | **Base Address + Offset** |
| --- | --- |
| DMA\_CONTROL\_REG | 0x00 |
| DMA\_STATUS\_REG | 0x04 |
| DMA\_COMMAND\_REG | 0x08 |
| DMA\_REQUEST\_REG | 0x0C |
| CH0\_BASE\_ADDR\_REG | 0x10 |
| CH0\_BASE\_WORD\_COUNT\_REG | 0x14 |
| CH0\_CONTROL\_REG | 0x18 |
| CH0\_CURRENT\_ADDR\_REG | 0x1C |
| CH0\_CURRENT\_WORD\_COUNT\_REG | 0x20 |
| CH0\_MASK\_REG | 0x24 |

These offsets make it easy for software or a CPU to configure or check the DMA channels individually

**1. Channel-Specific Registers (Each Channel: 0, 1, 2)**

**a. Source Address Register (CHn\_SRC\_ADDR)**

* **Address:** 0x4000\_0000 + n×0x18 (n=0/1/2, offset 0x00/0x18/0x30)
* **Offset per Channel:** 0x00 (CH0), 0x18 (CH1), 0x30 (CH2)
* **Width:** 32 bits
* **Bits:** [31:0] – Source start address for DMA transfer.
* **Function:** Where DMA reads data from for this channel.

**b. Destination Address Register (CHn\_DST\_ADDR)**

* **Address:** CHn\_SRC\_ADDR + 0x04
* **Offset:** 0x04, 0x1C, 0x34
* **Width:** 32 bits
* **Bits:** [31:0] – Destination start address.
* **Function:** Where DMA writes data for this channel.

**c. Word Count Register (CHn\_TRANS\_SIZE)**

* **Address:** CHn\_SRC\_ADDR + 0x08
* **Offset:** 0x08, 0x20, 0x38
* **Width:** 32 bits
* **Bits:** [31:0] – Number of data units (bytes/words) to transfer.
* **Function:** How many units DMA will move for this transfer.

**d. Control Register (CHn\_CTRL)**

* **Address:** CHn\_SRC\_ADDR + 0x0C
* **Offset:** 0x0C, 0x24, 0x3C
* **Width:** 8 bits
* **Bits:**
  + - Enable (1=start, 0=stop)
  + - Src Address Increment (1=inc, 0=fixed)
  + - Dst Address Increment (1=inc, 0=fixed)
  + - Data Width (0=8bit, 1=32bit)
  + - Burst Mode (0=single, 1=burst)
  + - Interrupt Enable
  + [7:6] - Reserved (set to 0)
* **Function:** Configures and starts DMA transfer per channel.

**e. Status Register (CHn\_STATUS)**

* **Address:** CHn\_SRC\_ADDR + 0x10
* **Offset:** 0x10, 0x28, 0x40
* **Width:** 8 bits
* **Bits:**
  + - Active (1=busy, 0=idle)
  + - Transfer Complete (auto-clear/write 1 to clear)
  + - Error
  + [7:3] - Reserved
* **Function:** Reports DMA status. Cleared by software.

**f. Interrupt Register (CHn\_INT)**

* **Address:** CHn\_SRC\_ADDR + 0x14
* **Offset:** 0x14, 0x2C, 0x44
* **Width:** 3 bits
* **Bits:**
  + – Interrupt Pending (read/clear)
  + – Interrupt Enable (mirror of CTRL for ease)
  + – Error Interrupt Enable
* **Function:** Interrupt status/control per channel.

**2. Global Registers**

**a. MASK Register (DMAC\_MASK)**

* **Address:** 0x4000\_0048
* **Offset:** 0x48
* **Width:** 3 bits
* **Bits:**
  + [2:0] CH2, CH1, CH0: (1=mask/disable INT/req, 0=enable)
* **Function:** Masks/unmasks DMA interrupts or requests globally.

**b. REQUEST Register (DMAC\_REQ)**

* **Address:** 0x4000\_004C
* **Offset:** 0x4C
* **Width:** 3 bits
* **Bits:**
  + [2:0] CH2, CH1, CH0: (write 1 to trigger SW request)
* **Function:** Software can trigger a DMA transfer per channel.

**c. COMMAND Register (DMAC\_CMD)**

* **Address:** 0x4000\_0050
* **Offset:** 0x50
* **Width:** 8 bits
* **Bits:**
  + – Global Start (1=Start all enabled channels)
  + – Global Stop (1=Halt all)
  + – Global Reset
  + [7:3] – Reserved (0)
* **Function:** Global DMA controller actions.

**d. CONTROL Register (DMAC\_CTRL)**

* **Address:** 0x4000\_0054
* **Offset:** 0x54
* **Width:** 8 bits
* **Bits:**
  + – Global Enable (DMA system on/off)
  + [2:1] – Arbitration Mode (00=RR, 01=fixed)
  + [7:3] – Reserved (0)
* **Function:** Top-level settings for the DMAC.